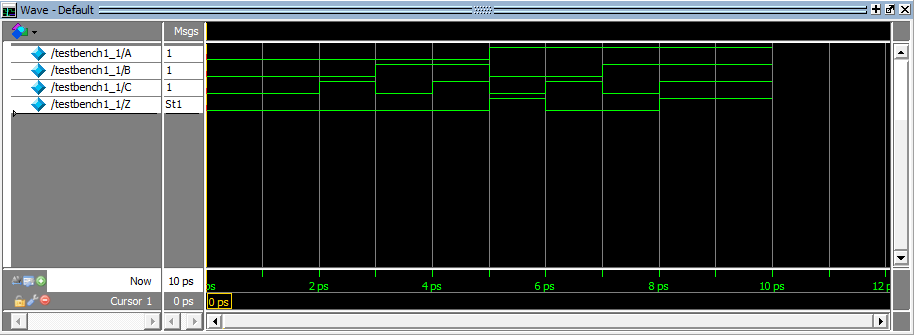
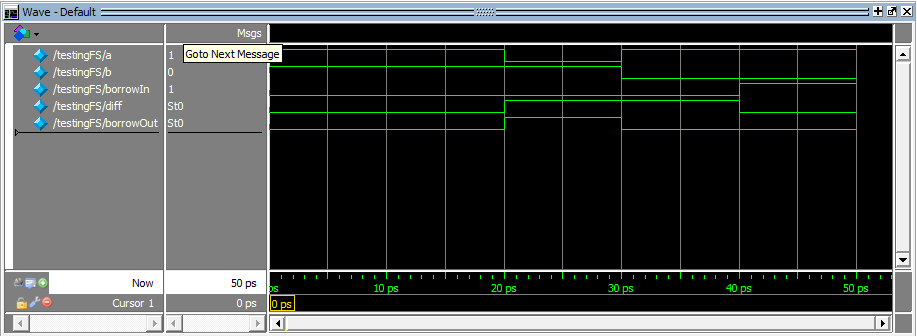
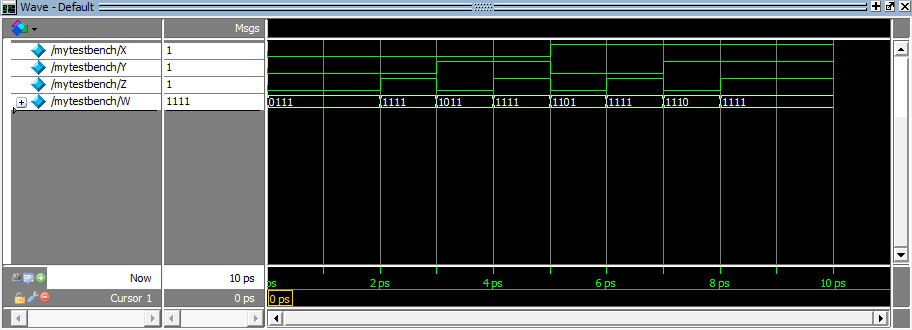
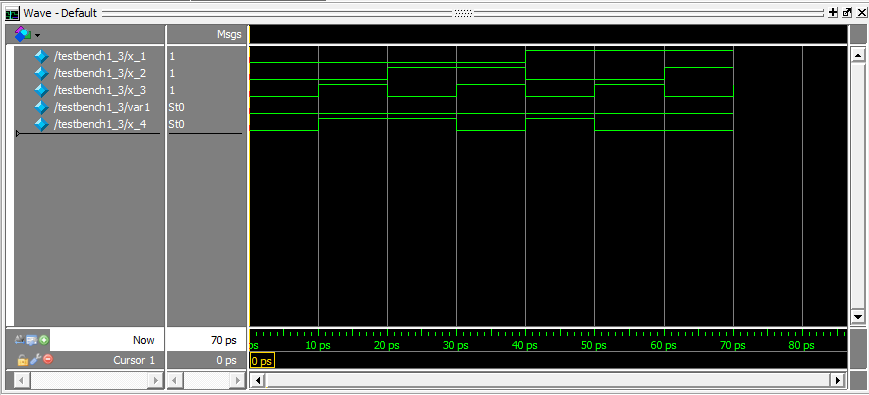
DRILL 1

* **Drill1\_1.v Testbench**
* **Drill1\_2.v Testbench**
* **Exercise1\_1.v Testbench**
* **Exercise1\_3.v Testbench**

**Review Questions**

1. **Based from Drill1\_1, notice that wire1, wire2, and wire3 are outputs of gates EOR2, NOT and AND2 respectively. Why are they declared as wire instead of output?**

*Because the wire1, wire2, wire3 are not the final output of the module they are internals nets used to interconnect components within the module and form the final output.*

1. **How do you instantiate a module within a test bench?**

*To instantiate a module within a test bench by typing the* ***“module name”*** *and next to it is the* ***“instance name”*** *which is a unique identifier for the instance of the module and after that are the* ***“port list”*** *within parathesis.*

***<module\_name> <identifier> (<port\_list>);***

1. **Can we instantiate a test bench from another test bench? Why or why not?**

*No, we can’t instantiate a testbench from another testbench since testbench is a special type of module that is used to instantiate or test the modules. If you try to instantiate testbench in another testbench it will cause syntax error/compilation error.*